cadence

Fast and Accurate Phase Noise Analysis of Crystal Oscillator in 28 FDSOI Process

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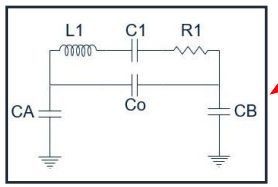
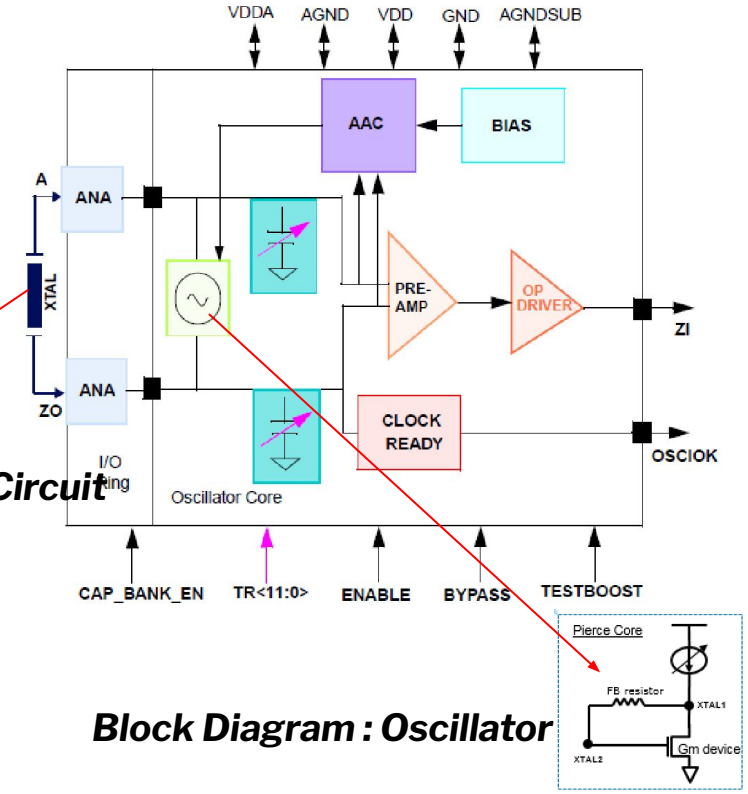
Motivation

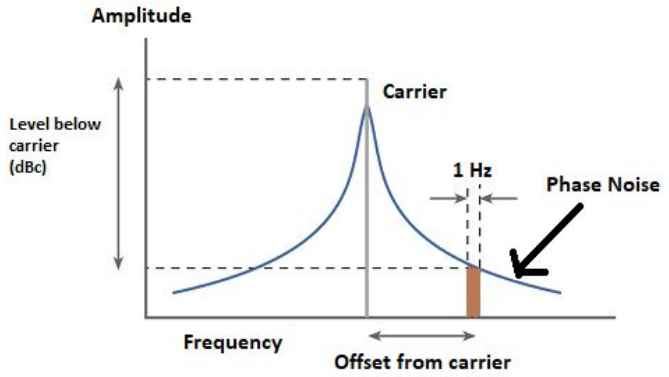
- Phase noise of Crystal(XTAL) Oscillator is important as it acts as the reference for the PLL, thus best phase noise is targeted for the XTAL Oscillator.
- Due to High Q & very low noise levels of the XTAL, computation of phase noise accurately is a challenge.
- Designed XTAL oscillator is required to provide 50MHz as a reference clock to the PLL with target phase noise of < -168 dBc/Hz @100 kHz offset & < -173 dBc/Hz @1 MHz offset (SSB) across PVT.
- For XTAL oscillators, the frequency and amplitude of the harmonics is solved using Harmonic Balance (HB) analysis which is a frequency domain analysis that helps in determining the steady-state behavior of oscillator.



XTAL Equivalent Circuit



Block Diagram : Oscillator



Generic Phase Noise Plot

Noise Filtering of Major Contributors

XTAL Core

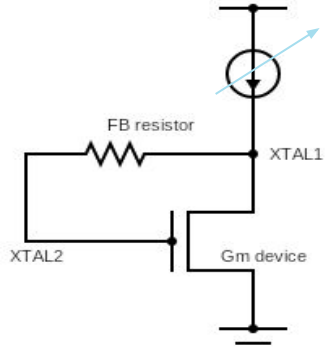
- Used Pierce architecture to generate highly accurate frequency & good phase noise.
- Efficiently designed Automatic Amplitude Control to generate targeted phase noise at XTAL core.

AAC, Bandgap, Biasing circuitry

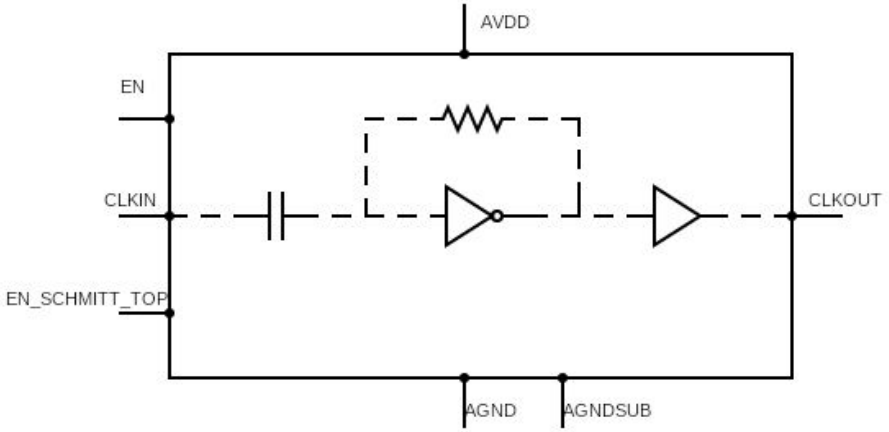
- Noise Filtered using the RC Filter.

Level Shifter

- Used AC Coupled level shifter to mitigate the noise degradation due to level shifter.



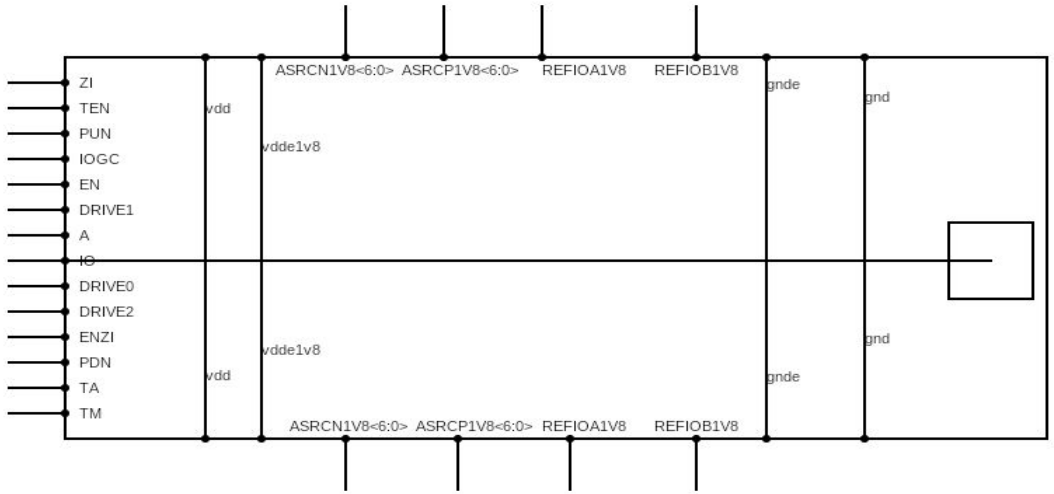
Pierce Architecture



Level Shifter

Impact of IO's on the Phase Noise

- To compare with the results measured at Silicon, contribution due to IO pad was critical.
- Lower drive levels of the IO was significantly degrading the phase noise at the measurable output .
- With higher drive strength IO's, phase noise was improved at the output confirming the reference clock to the PLL has the desired target phase noise.



IO PAD

Challenges/Requirements

- In steady state analysis, the number of harmonics and oversample have a larger effect on accuracy therefore, convergence issues are faced most of the times in simulator which results in multiple iterations, longer simulation time and overall productivity impact.

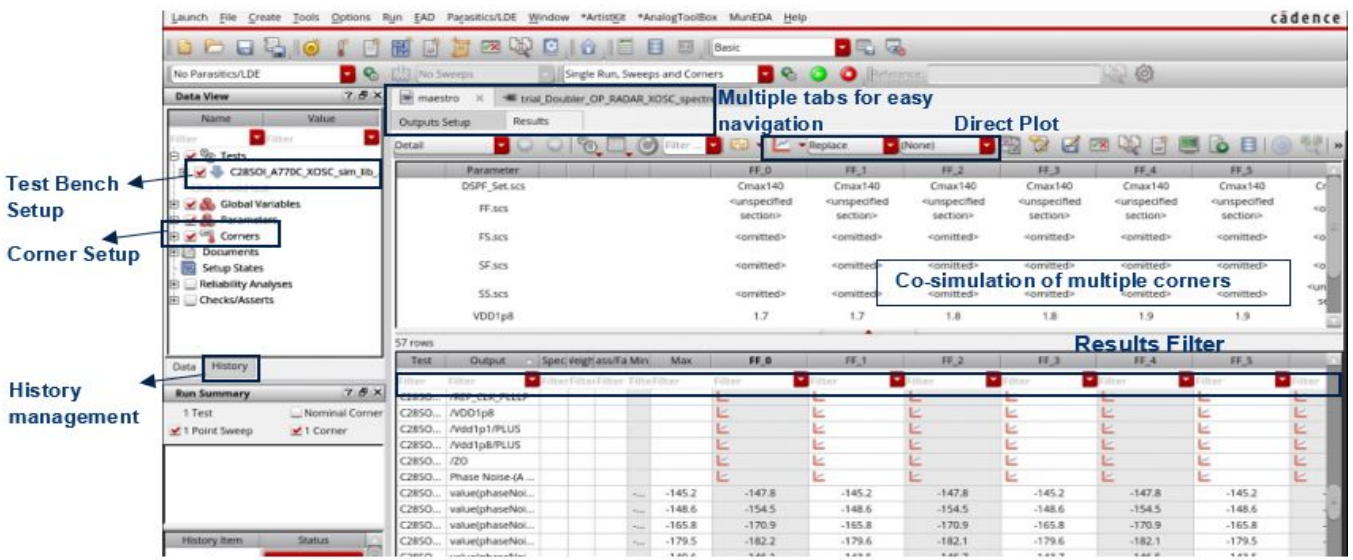
- To address above challenges, the simulator should suffice below requirements.
  - Accurate phase noise results
  - Able to run simulations across multiple variables and PVTs using single Interface.
  - Consistent simulator settings across the simulations.
  - Less convergence issues.
  - Easy/quick debugging and postprocessing of results.
  - Effective sharing and re-usability of design/setups and results.

Proposed Methodology

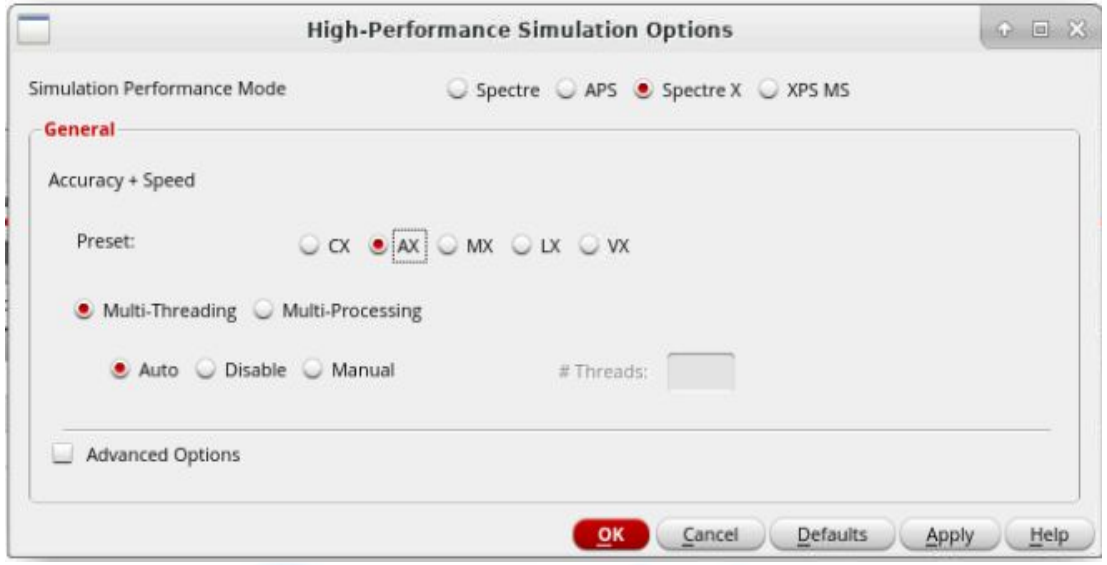
- With multiple features of Cadence Virtuoso ADE-Assembler like, Co-simulating multiple test setups in single maestro view, use of filters in sorting of results, simple corner setup, direct plotting etc. helps in productivity gain, enhances the reusability of setup for various simulations.

- Automatic mapping between pre-layout output expressions and their corresponding DSPF syntax in Virtuoso ADE-Assembler allowed the use of same measurement expressions for pre- and post-layout simulations. This leads to significant reduction in turn-around time as there is no need to re-write all measurement expressions as per DSPF syntax.

- Convergence and simulation performance challenges addressed by using Cadence Spectre X-RF option.



ADE Assembler GUI

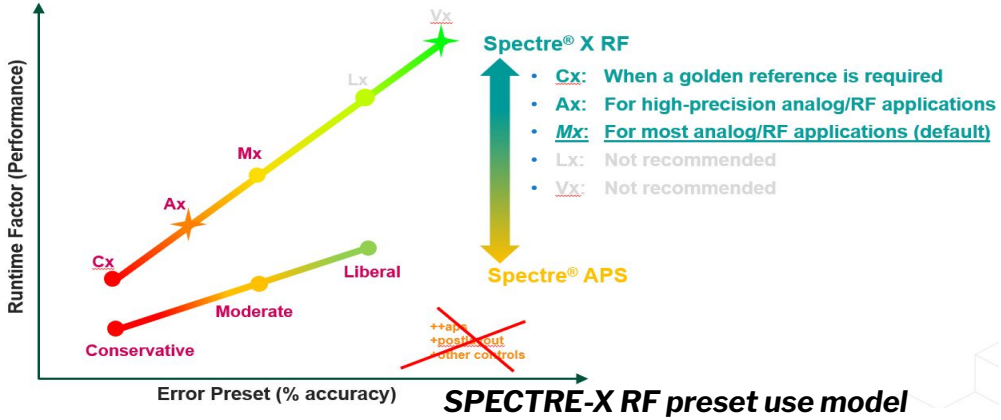


SPECTRE-X GUI in ADE

Spectre X-RF option

- Enabled Spectre X technology for RF Analysis for Shooting Newton(pss) and Harmonic Balance (HB) analysis.
- Spectre X-RF option provides simple single-preset use model with various modes (CX, AX, MX) to control the accuracy thereby, eliminating the need to specify multiple additional simulator options.
- Spectre X-RF option has enhanced performance, capacity and optimized memory consumption as compared to existing solution.
- Seamless integration of Virtuoso ADE-Assembler and Spectre X-RF option greatly helped in optimizing the simulation setup and reducing the turn-around time by using features like, Auto detect-steady state, single hb-noise setup for multiple nets, disabling noise contribution for a particular instance in the schematic.

When a golden reference is required	Start with +preset=cx
New Design	Start with +preset=ax
Design too big/long for APS	Start with +preset=mx



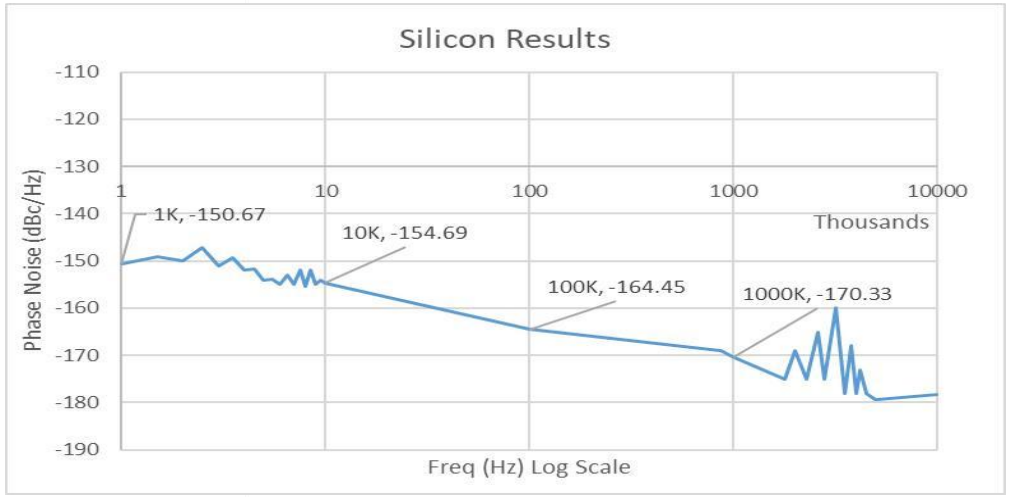
SPECTRE-X RF preset use model

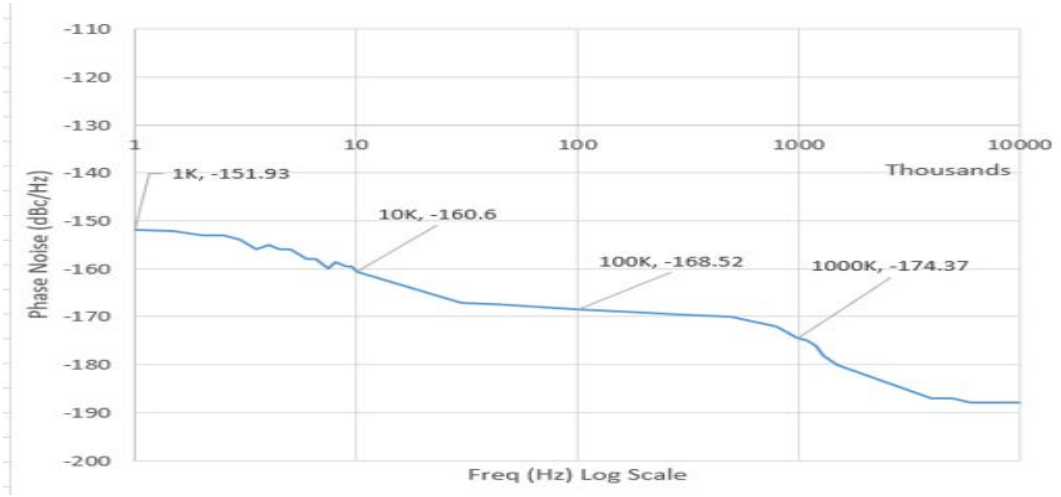
APS to Spectre X Migration

APS setting	+/++aps=conservative +postlayout=upa	+aps=moderate +postlayout=hpa	++moderate / +liberal +postlayout=hpa
SpectreX preset	CX	AX	MX

Results

- Results computed by CAD (SPECTRE X) were close to the Silicon results across multiple frequency offsets.





SSB Silicon Results

SSB Spectre-X AX mode Results

	Freq. Offset	Silicon	Existing Solution	Spectre-X (+preset=AX)
SSB Phase Noise	1K	-150.67dBc/Hz	-151.87Bc/Hz	-151.93dBc/Hz
	10K	-154.69dBc/Hz	-160.58Bc/Hz	-160.6dBc/Hz
	100K	-164.45dBc/Hz	-169.66Bc/Hz	-168.52dBc/Hz
	1M	**-170.33dBc/Hz**	**-174.73Bc/Hz**	**-174.37dBc/Hz**
	Simulation Time	**-**	**3hr16min**	**1hr41min**
	Performance Gain			~2X

Summary

- Crystal Oscillator being a **High Q** circuit, convergence issues are being addressed by Spectre-X RF.
- Using **+preset=AX** of Spectre X-RF option gives performance gain of **~2X** as compared to existing solution**.**
- Achieved Silicon accuracy.
- Seamlessly integrated Virtuoso ADE-Assembler Spectre-X RF option flow reduced the overall design time by **30%**